REMARKS

Prior to entry of the present Amendment, claims 1 and 27-92 were pending in the present application. Claims 27-46, 72, 73 and 75-92 are amended above. Claims 1, 47-71 and 74 are cancelled above. New claims 93-95 are added above. No new matter is added by the claim amendments or new claims. Entry is respectfully requested.

The Applicants note that an updated Office Action was mailed by the Office on October 15, 2005. With reference to the inquiry at page 2, paragraph 1 of the updated Office Action, the Applicants confirm that no response was filed on July 28, 2005. The Applicants further note that the time for response has been reset by the updated Office Action to three months from October 18, 2005, or January 18, 2006.

The specification is amended to correct a clerical error.

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicants further note that the Preliminary Amendment filed with the application papers on October 30, 2003 has not been acknowledged. The Preliminary Amendment cancelled claims 2-26.

Claims 32-34 stand rejected under 35 U.S.C. 112, second paragraph. Claims 32-34 are amended to depend from claim 30. Entry of the amendments and removal of the rejections are respectfully requested.

Claims 27-37, 41-43, 45-46, 72-83, 87-89 and 91-92 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama (U.S. Patent Number 6,548,875). Claims 38-40

and 84-86 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama in view of Liu (U.S. Patent Number 6,528,847). Claims 44 and 90 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama in view of Lee, *et al.* (U.S. Patent Number 6,376,318). Reconsideration of the rejection and allowance of claims 27-46 and 72-92 are respectfully requested.

In the present invention as claimed in claim 27, a MOS transistor having an elevated source and drain structures includes a "gate electrode" on a "gate dielectric layer" and "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the gate dielectric layer in a horizontal direction substantially parallel to the substrate". "First source/drain regions" are formed in the "epitaxial layer adjacent the gate dielectric layer at lower side portions of the gate electrode". "Insulating sidewall spacers" are formed "having bottom portions on the first source/drain regions in the epitaxial layer at an upper side portion of the gate electrode".

Independent claim 27 is amended to clarify certain features of the invention. Specifically, the claim is amended to recite that the MOS transistor having elevated source and drain structures includes "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the gate dielectric layer in a horizontal direction substantially parallel to the substrate". Claim 27 is further amended to recite that the MOS transistor having elevated source and drain structures includes "insulating sidewall spacers having bottom portions on the first source/drain regions in the epitaxial layer". It is believed that these claim amendments clarify the distinctions between the invention and the cited references.

In the present invention as claimed in claim 72, a MOS transistor having elevated source and drain structures includes a "gate electrode" on a "gate dielectric layer", the "gate dielectric layer includes a horizontal portion that extends across a bottom portion of the gate electrode and vertical portions that extend along lower side portions of the gate electrode", and "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the

vertical portions of the gate dielectric layer in a horizontal direction substantially parallel to the substrate".

Independent claim 72 is amended to clarify certain features of the invention. Specifically, the claims are amended to recite that the MOS transistor having elevated source and drain structures includes the "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the vertical portions of the gate dielectric layer in a horizontal direction substantially parallel to the substrate". It is believed that these claim amendments clarify the distinctions between the invention and the cited references.

Nishiyama discloses a gate electrode 216 formed on a gate insulation film 204 extending under the gate electrode and gate sidewalls 208 that extend over the entire sidewalls of the gate electrode. Source/drain electrodes are formed in recesses of source/drain semiconductor layers 212. The source/drain semiconductor layers 212 extend from bottom corners of the gate sidewalls 208 at an angle. An SiO_2 film (second dielectric film) 215 is provided as a layer to fill a void between the source/drain semiconductor layers 212 and the gate insulation film 204 and gate sidewalls 208.

With regard to the rejection of independent claim 27, Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the gate dielectric layer in a horizontal direction substantially parallel to the substrate", as claimed in claim 27. Instead, in Nishiyama, the source/drain semiconductor layers 212 extend from the gate sidewalls 208 at an angle. Further, Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes "insulating sidewall spacers having bottom portions on the first source/drain regions in the epitaxial layer", as claimed in claim 27. Instead, in Nishiyama, the SiO_2 film 215 is not a sidewall spacer but rather a void-filling insulative region. In addition, the gate sidewalls 208 of Nishiyama are not formed on the source/drain semiconductor layers 212, thus failing to teach or suggest "having bottom portions on the first

source/drain regions in the epitaxial layer", as claimed in claim 27.

With regard to the rejection of independent claim 72, Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes a "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the vertical portions of the gate dielectric layer in a horizontal direction substantially parallel to the substrate", as claimed in claim 72. Instead, in Nishiyama, the source/drain semiconductor layers 212 extend from the gate sidewalls 208 at an angle. Further, Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes "a gate dielectric layer that includes a horizontal portion that extends across a bottom portion of the gate electrode and vertical portions that extend along lower side portions of the gate electrode", as claimed in claim 72. The only portion of the Nishiyama gate structure that is formed as a dielectric layer is the gate insulation film layer 204 that lies below the gate 205. The gate sidewalls 208 of Nishiyama at side portions of the gate are not a "gate dielectric layer", as claimed.

It is therefore submitted that independent claims 27 and 72 are allowable over Nishiyama. Reconsideration of the rejection of claims 27 and 72 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama, and allowance of the claims, are respectfully requested. With regard to the rejection of dependent claims 28, 29, 31-37, 41-43, 45-46, 73-75, 77-83, 87-89, and 91-92 as being unpatentable over Nishiyama, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of claims 38-40 and 84-86 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Liu are respectfully requested, Liu is cited in the Office Action as disclosing a recessed channel. Liu discloses a polysilicon gate 36 formed on gate oxide layer 34, and spacers 60 formed on the gate oxide layer 34. Liu fails to teach or suggest an epitaxial layer, thus, like Nishiyama, Liu fails to teach or suggest a MOS transistor having elevated source and drain structures that includes "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the gate dielectric layer in a horizontal

direction substantially parallel to the substrate" and "insulating sidewall spacers having bottom portions on the first source/drain regions in the epitaxial layer", as claimed in claims 38-40. Like Nishiyama, Liu further fails to teach or suggest a MOS transistor having elevated source and drain structures that includes a "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the vertical portions of the gate dielectric layer in a horizontal direction substantially parallel to the substrate", as claimed in claims 84-86. Accordingly, it is submitted that the combination of Nishiyama and Liu fails to teach or suggest the invention as claimed in claims 38-40 and 84-86. Reconsideration of the rejection of, and allowance of, claims 38-40 and 84-86 are respectfully requested.

With regard to the rejection of claims 44 and 90 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Lee, *et al.*, Lee, *et al.* is cited in the Office Action as disclosing an oxide film spacer 27. Lee, *et al.* discloses a nitride film spacer 28 formed adjacent the oxide film spacer 27 and a selective epitaxial growth film 29 which forms a self aligned epitaxial silicon sliver (SESS) C adjacent the oxide film spacer 27 and under the nitride film spacer 28.

Like Nishiyama, Lee, *et al.* fail to teach or suggest a MOS transistor having elevated source and drain structures that includes "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the gate dielectric layer in a horizontal direction substantially parallel to the substrate", as claimed in claim 44. Instead, in Lee, *et al.*, there is no dielectric layer for the epitaxial layer to contact. Further, like Nishiyama, Lee, *et al.* fails to teach or suggest "insulating sidewall spacers having bottom portions on the first source/drain regions in the epitaxial layer", as claimed in claim 44. Instead, in Lee, *et al.*, neither the oxide film spacers 27 nor the nitride film spacers are formed on "source/drain regions in the epitaxial layer". Like Nishiyama, Lee, *et al.* further fails to teach or suggest a MOS transistor having elevated source and drain structures that includes a "an epitaxial layer contacting a side portion of the gate dielectric layer on the substrate and extending from the vertical portions of the gate dielectric layer in a horizontal direction substantially parallel to the substrate", as claimed in claim 90. Instead, in Lee, *et al.*, there is no dielectric layer for the epitaxial layer to contact.

Accordingly, it is submitted that the combination of Nishiyama and Lee, *et al.* fails to teach or suggest the invention as claimed in claims 44 and 90. Reconsideration of the rejection of, and allowance of, claims 44 and 90, are respectfully requested.

With regard to the newly added claims 93-128, it is submitted that the cited references, whether alone or in combination, fail to teach or suggest the invention as claimed. Entry and allowance are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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